Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SANJAY R. DESHPANDE

Appeal No. 1999-2286
Application No. 08/352,660

ON BRIEF

Before FLEMING, BARRY, and LEVY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from an examiner's rejection of claims 1-7, 9, and 10. We reverse.

BACKGROUND

The invention at issue in this appeal is a protocol for arbitrating control of a bus between first and second subsystems coupled thereto. Bus arbitration protocols are well known in the art. A symmetrical protocol uses three clock cycles. The first cycle is used for a request; the

second cycle is used for arbitration; and the third cycle is used for a response.

The appellant seeks to reduce the number of clock cycles used to access a common bus. Using an asymmetrical protocol, the first, i.e., priority, subsystem has a zero latency in accessing the bus, while the second subsystem must wait at least one clock cycle after the first subsystem relinquishes control of the bus. More specifically, the first subsystem transmits both a request to transmit data and data substantially simultaneously. Thereafter, the second subsystem is granted access to the bus one cycle after requesting access to the bus after the first subsystem has completed its transmission. Similarly, the first subsystem regains control of the bus one cycle after requesting access to the bus after the second subsystem has completed its transmission.

Claim 7, which is representative for present purposes, follows:

> 7. A synchronous communication system comprising a plurality of subsystems coupled to a system bus, each subsystem further comprising a [sic] unidirectional control line coupled to the rest of said plurality of subsystems whereby asymmetrical control of said bus is arbitrated between a first subsystem and a second subsystem based upon control signals communicated one to another over said control lines and through a transparent latch within each of said first and second subsystems, each transparent latch being coupled to
>
> said control lines, and said first subsystem transmitting a request and data substantially simultaneously, said request being transmitted during said transmission of said data.

The prior art applied by the examiner in rejecting the claims follows:

> May et al. (May) 4,811,277 Mar. 7, 1989
>
> Craft et al. (Craft) 4,987,529 Jan. 22, 1991
>
> Nakada et al. (Nakada), Bus Arbitration Method for a Two-Way Multiprocessor, IBM Technical Disclosure Bulletin, Oct. 1992, at 439-42.

Claims 1-7 and 9 stand rejected under 35 U.S.C. § 103 as being obvious over Nakada in view of Craft. (Examiner's Answer, ¶ 9.) Claim 10 stands rejected under § 103 as being obvious over Nakada in view of Craft further in view of May. (Id.)

Rather than reiterate the arguments of the appellant or examiner in toto, we refer the reader to the briefs and answers for the respective details thereof.

OPINION

After considering the record, we are persuaded that the examiner erred in rejecting claims 1-7, 9, and 10. Accordingly, we reverse. We begin by summarizing the examiner's rejection and the appellant's argument.

The examiner asserts that Nakada's "processor 1 would transmit the data to the processor 2 via the bus and also request the processor 2 to transmit the data back by using the BREQ (bus request) substantially simultaneously (see page 440-441 and fig. 1)." (Supplemental Examiner's Answer at 2.) The appellant argues, "[t]he first processor does not transmit a request to use the bus simultaneously with the data to be transmitted." (Reply Br. at 4.)

Claims 1-6 specify in pertinent part the following limitations: "allowing said first subsystem to transmit said

request and data substantially simultaneously, said request being transmitted during said transmission of said data ...." Similarly, claims 7, 9, and 10 specify in pertinent part the following limitations: "said first subsystem transmitting a request and data substantially simultaneously, said request being transmitted during said transmission of said data." Accordingly, claims 1-7, 9, and 10 require inter alia a first subsystem transmitting a request to use a bus substantially simultaneously with data to be transmitted on the bus.

The examiner fails to show a teaching or suggestion of the limitations in the applied prior art. "'A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.'" In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, Nakada teaches that a first processor transmits a request to use a bus. Specifically, "[w]hen Processor 1 needs

to use the bus, it activates BREQ to ask Processor 2 to release the bus." P. 441. The request, however, is not transmitted substantially simultaneously with data to be transmitted on the bus. To the contrary, after activating BREQ, Processor 1 must wait for Processor 2 to complete its transmission before beginning to transmit data. Specifically, "[w]hen BREQ is activated, Processor 2 releases the bus and deactivates HOLD after completing the current outstanding bus operations." Id.

Relying on Craft to teach that "bus arbitration grants the control of the shared bus to the bus masters or other requesters having the highest priority," (Examiner's Answer at 3), and May to teach "a clock signal ... coupled to the first and second subsystems ... for providing synchronization between the subsystems," (id. at 6), the examiner fails to allege, let alone show, that the additional references cure the defect of Nakada. Because the latter reference's Processor 1 must wait for Processor 2 to complete its transmission before beginning to transmit data, we are not persuaded that the teachings from the applied prior art would

have suggested the limitations of "allowing said first subsystem to transmit said request and data substantially simultaneously, said request being transmitted during said transmission of said data" or "said first subsystem transmitting a request and data substantially simultaneously, said request being transmitted during said transmission of said data." Therefore, we reverse the rejection of claims 1-7 and 9 as being obvious over Nakada in view of Craft and of claim 10 as being obvious over Nakada in view of Craft further in view of May.

CONCLUSION

In summary, the rejection of claims 1-7, 9, and 10 under § 103 is reversed.

REVERSED

MICHAEL R. FLEMING Administrative Patent Judge	)	
LANCE LEONARD BARRY Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)	

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